

## WHAT IS CLAIMED IS:

1           1.     For use with a clocked circuit, a clock selection circuit  
2     capable of receiving a first input clock signal and a second input  
3     clock signal and outputting to said clocked circuit a selected  
4     clock signal derived from one of said first and second input clock  
5     signals, said clock selection circuit comprising:

6                 a first clock control circuit that receives said first  
7     input clock signal and a first start signal, wherein said first  
8     start signal, when asserted, is capable of causing said first clock  
9     control circuit to output a first gated clock signal;

10                a second clock control circuit that receives said second  
11    input clock signal and a second start signal, wherein said second  
12    start signal, when asserted, is capable of causing said second  
13    clock control circuit to output a second gated clock signal;

14                a first interlock circuit that detects when said first  
15    clock control circuit begins outputting said first gated clock  
16    signal and, in response to said detection, that asserts a first  
17    disable signal capable of preventing said second clock control  
18    circuit from outputting said second gated clock signal;

19                a second interlock circuit that detects when said second  
20    clock control circuit begins outputting said second gated clock  
21    signal and, in response to said detection, that asserts a second

22     disable signal capable of preventing said first clock control  
23     circuit from outputting said first gated clock signal; and  
24             a first OR gate that receives said first and second gate  
25     clock signal and outputs said selected clock signal.

1             2.     The clock selection circuit as set forth in Claim 1  
2     wherein said first interlock circuit detects when said first clock  
3     control circuit stops outputting said first gated clock signal and,  
4     in response to said detection, de-asserts said first disable signal  
5     after a first delay period suitable to allow a clock pulse  
6     propagating through said first clock control circuit to be  
7     completely output at said selected clock signal.

1           3.    The clock selection circuit as set forth in Claim 2  
2    wherein said a first clock control circuit comprises:

3               a first clock enable circuit that receives said second  
4    disable signal and said first start signal and outputs a first  
5    clock enable signal when said first start signal is asserted and  
6    said second disable signal is not asserted; and

7               a first AND gate having a first input coupled to said  
8    first clock enable signal and a second input coupled to said first  
9    input clock signal, wherein said first AND gate outputs said first  
10   gated clock signal.

1           4.    The clock selection circuit as set forth in Claim 3  
2    wherein said first clock enable circuit comprises a first input  
3    logic circuit having an output that outputs a Logic 1 when said  
4    first start signal is asserted and said second disable signal is  
5    not asserted.

1           5. The clock selection circuit as set forth in Claim 4  
2 wherein said first clock enable circuit further comprises a first  
3 flip-flop having an input coupled to said output of said first  
4 input logic circuit, wherein said first flip-flop is clocked by a  
5 rising edge of said first input clock signal and said first  
6 interlock circuit monitors an output of said first flip-flop to  
7 detect when said first clock control circuit begins outputting said  
8 first gated clock signal.

1           6. The clock selection circuit as set forth in Claim 5  
2 wherein said first clock enable circuit further comprises:

3               a second flip-flop having an input coupled to said output  
4 of said first flip flop, wherein said second flip-flop is clocked  
5 by a falling edge of said first input clock signal; and

6               a second OR gate having a first input coupled to said  
7 output of said first flip-flop and a second input coupled to an  
8 output of said second flip-flop, wherein an output of said second  
9 OR gate comprises said first clock enable signal.

1           7. The clock selection circuit as set forth in Claim 6  
2 wherein said second interlock circuit detects when said second  
3 clock control circuit stops outputting said second gated clock  
4 signal and, in response to said detection, de-asserts said second  
5 disable signal after a delay period suitable to allow a clock pulse  
6 propagating through said second clock control circuit to be  
7 completely output at said selected clock signal.

1           8. The clock selection circuit as set forth in Claim 7  
2 wherein said a second clock control circuit comprises:

3           a second clock enable circuit that receives said first  
4 disable signal and said second start signal and outputs a second  
5 clock enable signal when said second start signal is asserted and  
6 said first disable signal is not asserted; and

7           a second AND gate having a first input coupled to said  
8 second clock enable signal and a second input coupled to said  
9 second input clock signal, wherein said second AND gate outputs  
10 said second gated clock signal.

1           9. The clock selection circuit as set forth in Claim 8  
2 wherein said second clock enable circuit comprises a second input  
3 logic circuit having an output that outputs a Logic 1 when said  
4 second start signal is asserted and said first disable signal is  
5 not asserted.

1           10. The clock selection circuit as set forth in Claim 9  
2 wherein said second clock enable circuit further comprises:

3           a third flip-flop having an input coupled to said output  
4 of said second input logic circuit, wherein said third flip-flop is  
5 clocked by a rising edge of said second input clock signal and said  
6 second interlock circuit monitors an output of said third flip-flop  
7 to detect when said second clock control circuit begins outputting  
8 said second gated clock signal;

9           a fourth flip-flop having an input coupled to said output  
10 of third flip-flop, wherein said fourth flip-flop is clocked by a  
11 falling edge of said second input clock signal; and

12           a third OR gate having a first input coupled to said  
13 output of said third flip-flop and a second input coupled to an  
14 output of said fourth flip-flop, wherein an output of said third OR  
15 gate comprises said second clock enable signal.

1 11. A processing system comprising:

2 a clocked circuit capable of operating at a plurality of  
3 clock frequencies;

4 a first clock signal source;

5 a second clock signal source;

6 a clock selection circuit capable of receiving a first  
7 input clock signal from said first clock signal source and a second  
8 input clock signal from said second clock signal source and  
9 outputting to said clocked circuit a selected clock signal derived  
10 from one of said first and second input clock signals, said clock  
11 selection circuit comprising:

12 a first clock control circuit that receives said  
13 first input clock signal and a first start signal, wherein  
14 said first start signal, when asserted, is capable of causing  
15 said first clock control circuit to output a first gated clock  
16 signal;

17 a second clock control circuit that receives said  
18 second input clock signal and a second start signal, wherein  
19 said second start signal, when asserted, is capable of causing  
20 said second clock control circuit to output a second gated  
21 clock signal;

22 a first interlock circuit that detects when said



23 first clock control circuit begins outputting said first gated  
24 clock signal and, in response to said detection, that asserts  
25 a first disable signal capable of preventing said second clock  
26 control circuit from outputting said second gated clock  
27 signal;

28 a second interlock circuit that detects when said  
29 second clock control circuit begins outputting said second  
30 gated clock signal and, in response to said detection, that  
31 asserts a second disable signal capable of preventing said  
32 first clock control circuit from outputting said first gated  
33 clock signal; and

34 a first OR gate that receives said first and second  
35 gate clock signal and outputs said selected clock signal.

1           12. The processing system as set forth in Claim 11 wherein  
2       said first interlock circuit detects when said first clock control  
3       circuit stops outputting said first gated clock signal and, in  
4       response to said detection, de-asserts said first disable signal  
5       after a first delay period suitable to allow a clock pulse  
6       propagating through said first clock control circuit to be  
7       completely output at said selected clock signal.

1           13. The processing system as set forth in Claim 12 wherein  
2       said a first clock control circuit comprises:

3           a first clock enable circuit that receives said second  
4       disable signal and said first start signal and outputs a first  
5       clock enable signal when said first start signal is asserted and  
6       said second disable signal is not asserted; and

7           a first AND gate having a first input coupled to said  
8       first clock enable signal and a second input coupled to said first  
9       input clock signal, wherein said first AND gate outputs said first  
10      gated clock signal.

1           14. The processing system as set forth in Claim 13 wherein  
2       said first clock enable circuit comprises a first input logic  
3       circuit having an output that outputs a Logic 1 when said first  
4       start signal is asserted and said second disable signal is not  
5       asserted.

1           15. The processing system as set forth in Claim 14 wherein  
2       said first clock enable circuit further comprises a first flip-flop  
3       having an input coupled to said output of said first input logic  
4       circuit, wherein said first flip-flop is clocked by a rising edge  
5       of said first input clock signal and said first interlock circuit  
6       monitors an output of said first flip-flop to detect when said  
7       first clock control circuit begins outputting said first gated  
8       clock signal.

1           16. The processing system as set forth in Claim 15 wherein  
2       said first clock enable circuit further comprises:

3           a second flip-flop having an input coupled to said output  
4       of said first flip flop, wherein said second flip-flop is clocked  
5       by a falling edge of said first input clock signal; and

6           a second OR gate having a first input coupled to said  
7       output of said first flip-flop and a second input coupled to an  
8       output of said second flip-flop, wherein an output of said second  
9       OR gate comprises said first clock enable signal.

1           17. The processing system as set forth in Claim 16 wherein  
2       said second interlock circuit detects when said second clock  
3       control circuit stops outputting said second gated clock signal  
4       and, in response to said detection, de-asserts said second disable  
5       signal after a delay period suitable to allow a clock pulse  
6       propagating through said second clock control circuit to be  
7       completely output at said selected clock signal.

1           18. The processing system as set forth in Claim 17 wherein  
2       said a second clock control circuit comprises:

3           a second clock enable circuit that receives said first  
4       disable signal and said second start signal and outputs a second  
5       clock enable signal when said second start signal is asserted and  
6       said first disable signal is not asserted; and

7           a second AND gate having a first input coupled to said  
8       second clock enable signal and a second input coupled to said  
9       second input clock signal, wherein said second AND gate outputs  
10      said second gated clock signal.

1           19. The processing system as set forth in Claim 18 wherein  
2       said second clock enable circuit comprises a second input logic  
3       circuit having an output that outputs a Logic 1 when said second  
4       start signal is asserted and said first disable signal is not  
5       asserted.

1           20. The processing system as set forth in Claim 19 wherein  
2       said second clock enable circuit further comprises:

3           a third flip-flop having an input coupled to said output  
4       of said second input logic circuit, wherein said third flip-flop is  
5       clocked by a rising edge of said second input clock signal and said  
6       second interlock circuit monitors an output of said third flip-flop  
7       to detect when said second clock control circuit begins outputting  
8       said second gated clock signal;

9           a fourth flip-flop having an input coupled to said output  
10      of third flip-flop, wherein said fourth flip-flop is clocked by a  
11      falling edge of said second input clock signal; and

12          a third OR gate having a first input coupled to said  
13      output of said third flip-flop and a second input coupled to an  
14      output of said fourth flip-flop, wherein an output of said third OR  
15      gate comprises said second clock enable signal.